BGS3510S
USB3.2 Gen1x1 Hub Controller

Datasheet

Revision 1.20

Oct. 12, 2023

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Revision History

Revision	Date	Description
1.00	02/01/2023	First release
1.10	09/28/2023	Update Electrical Characteristics
1.20	10/12/2023	Update Power Consumption

Table of Contents

1. General Description

BGS3510S is a USB3.2 Gen1x1 4-port HUB controller which is compliant with USB3.2 specification. It is fully backward compatible to USB2.0 and USB1.1 specification.

BGS3510S integrates self-developed USB 3.2 Gen 1x1 Super Speed transmitter/receiver physical layer (PHY) and USB 2.0 High-Speed PHY which has good signal integrity and compatibility. It also integrates 5V to 3.3V and 5V to 1.2V regulators which could the reduce BOM cost and ease the PCB design.

BGS3510S supports battery charging function for all downstream ports. It is compliant with USB Battery Charging specification rev1.2 and also supports charging various portable devices, such as Apple, Samsung Galaxy devices.

BGS3510S integrates USB2.0 HID/Billboard device and supports several interfaces, such as GPIOs, i2c master/slave and SPI. With these features, BGS3510S supports a variety of applications. And it

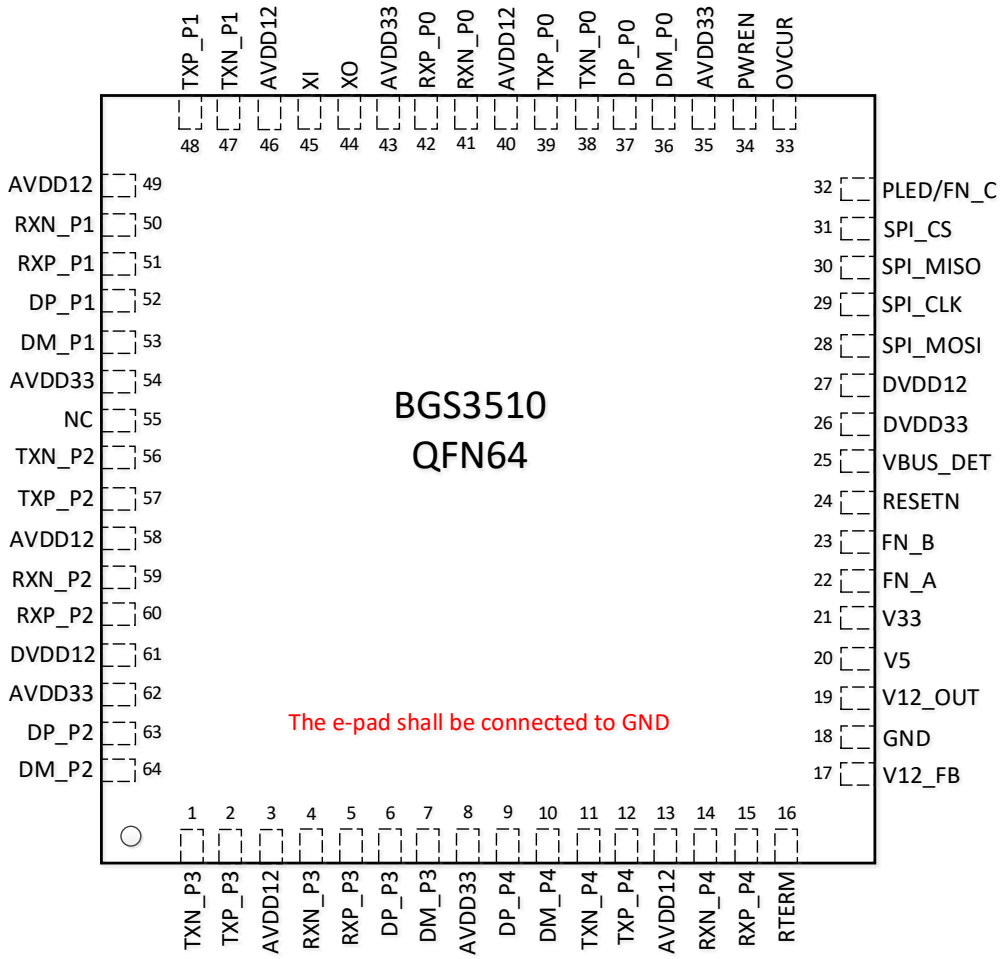
provides a framework for in-field firmware update and supports various customizations by updating firmware in external SPI flash.

2. Features

- Compliant with USB 3.2 Specification Revision 1.0
  - Upstream port supports Super-Speed, High-Speed and Full-Speed traffic
  - 4 downstream ports support Super-Speed, High-Speed, Full-Speed, and Low-Speed traffic
  - 1 control pipe and 1 interrupt pipe
  - Backward compatible to USB specification Revision 2.0 and 1.1
- Advanced power management and low power consumption
  - Support USB 3.2 Gen1x1 U0/U1/U2/U3 power management states
  - Support USB2.0 Link Power Management (LPM) L0/L1/L2
- MTT(Multiple Transaction Translator)
  - One TT for each downstream port.
  - Better data throughput when multiple downstream ports act on Full-Speed/Low-Speed concurrently.
- Compliant with USB Battery Charging Specification Revision 1.2 and other portable devices
  - Support BC1.2 Charging Downstream Port (CDP) mode
  - Support BC1.2 Dedicated Charging Port (DCP) mode
  - Support Apple 1A/2.1A/2.4A Charger mode (Divider Mode)
  - Support Samsung Galaxy devices fast-charging
- Flexible design
  - Support embedded USB2.0 HID or Billboard device
  - Support I2C master and I2C slave interface
  - Support Poly-fuse mode and Power Switch mode
  - Support Gang Mode and Individual Mode
  - Support external SPI flash for firmware upgrade
  - Support LED customize control
  - On-chip 8bit micro-processor
- Configurable settings
  - Support Efuse for function configure
  - Support GPIO pull control at PCB for function configure
- Low BOM cost
  - Single external 12 MHz crystal
  - Built-in upstream port 1.5KΩ pull-up and downstream port 15KΩ pull-down resistors
  - Built-in 5V to 3.3V and 5V to 1.2V regulator
- Application
  - USB hub/Docking station
  - Monitors/TV
  - Computer Systems
  - Set-Top Boxes

3. Pin Assignment

3.1 Pin-out Diagram



3.2 Pin Descriptions

Signal Type Definition

Name	Type	Description
Input	I	input-only signal
Output	O	output-only signal
Input/Output	I/O	bi-directional signal
Power	P	power/ground

Power/Ground Interface			
Pin Name	**Pin Number**	**I/O**	**Description**
AVDD12	3, 13, 40, 46, 49,58	P	1.2V power input for analog circuit
DVDD12	27, 61	P	1.2V power input for digital circuit
AVDD33	8, 35, 43, 54, 62	P	3.3V power input for analog circuit

DVDD33	26	P	3.3V power input for digital circuit
V33	21	P	5V-to-3.3V regulator 3.3V output and 3.3 input
V12_OUT	19	P	5V-to-1.2V DC-DC Switching regulator 1.2V output
V12_FB	17	P	5V-to-1.2V DC-DC Switching regulator feedback
V5	20	P	5V power input
GND	18	P	Ground

USB3.2 GEN1x1 Interface			
Pin Name	**Pin Number**	**I/O**	**Description**
TXN_P0 TXP_P0	38 39	O	USB3.2 Gen1x1 Differential Data Transmitter TX-/TX+ of Upstream Port
RXN_P0 RXP_P0	41 42	I	USB3.2 Gen1x1 Differential Data Receiver RX-/RX+ of Upstream Port
TXN_P1 TXP_P1	47 48	O	USB3.2 Gen1x1 Differential Data Transmitter TX-/TX+ of Downstream Port1
RXN_P1 RXP_P1	50 51	I	USB3.2 Gen1x1 Differential Data Receiver RX-/RX+ of Downstream Port1
TXN_P2 TXP_P2	56 57	O	USB3.2 Gen1x1 Differential Data Transmitter TX-/TX+ of Downstream Port2
RXN_P2 RXP_P2	59 60	I	USB3.2 Gen1x1 Differential Data Receiver RX-/RX+ of Downstream Port2
TXN_P3 TXP_P3	1 2	O	USB3.2 Gen1x1 Differential Data Transmitter TX-/TX+ of Downstream Port3
RXN_P3 RXP_P3	4 5	I	USB3.2 Gen1x1 Differential Data Receiver RX-/RX+ of Downstream Port3
TXN_P4 TXP_P4	11 12	O	USB3.2 Gen1x1 Differential Data Transmitter TX-/TX+ of Downstream Port4
RXN_P4 RXP_P4	14 15	I	USB3.2 Gen1x1 Differential Data Receiver RX-/RX+ of Downstream Port4

USB2.0 Interface			
Pin Name	**Pin Number**	**I/O**	**Description**
DM_P0 DP_P0	36 37	I/O	USB 2.0 DM/DP for Upstream Port
DM_P1 DP_P1	53 52	I/O	USB 2.0 DM/DP for Downstream Port1
DM_P2 DP_P2	64 63	I/O	USB 2.0 DM/DP for Downstream Port2
DM_P3 DP_P3	7 6	I/O	USB 2.0 DM/DP for Downstream Port3
DM_P4 DP_P4	10 9	I/O	USB 2.0 DM/DP for Downstream Port4
Hub Interface			

Pin Name	Pin Number	I/O	Description
PWREN	34	I/O	1. PWREN is the only power-enable output for GANG mode. 2. Strapping for Power Switch or PolyFuse • Pull high to support low-active power switch • Floating to support poly-fuse • Pull down to support high-active power switch
OVCUR	33	I/O	OVCUR is the only over current flag for GANG mode
VBUS_DET	25	I	Upstream VBUS power detection pin. Active High.
FN_A	22	I/O	For Downstream Port 3 Configuration • Floating to set downstream port 3 as non-removable port • Pull high no strapping
FN_B	23	I/O	For Downstream Port 4 Configuration • Pull down to disable downstream port 4 • Floating to set downstream port 4 as non-removable port • Pull high no strapping I2C SCL when configured as I2C Master/Slave
PLED/FN_C	32	I/O	1. PGANG LED 2. For Charger Configuration • Pull down to disable charging on all downstream ports • Pull high to enable charging on all downstream ports I2C SDA when configured as I2C Master/Slave

Clock and Reset Interface			
Pin Name	**Pin Number**	**I/O**	**Description**
XI	45	I	12M Crystal input. This pin is the crystal input for the internal oscillator. The input may alternately be driven by the output of an external oscillator. When using a crystal, a 1-MΩ feedback resistor is required between XI and XO.
XO	44	O	12M Crystal output. This pin is the crystal output for the internal oscillator. If XI is driven by an external oscillator this pin may be left unconnected. When using a crystal, a 1-MΩ feedback resistor is required between XI and XO.

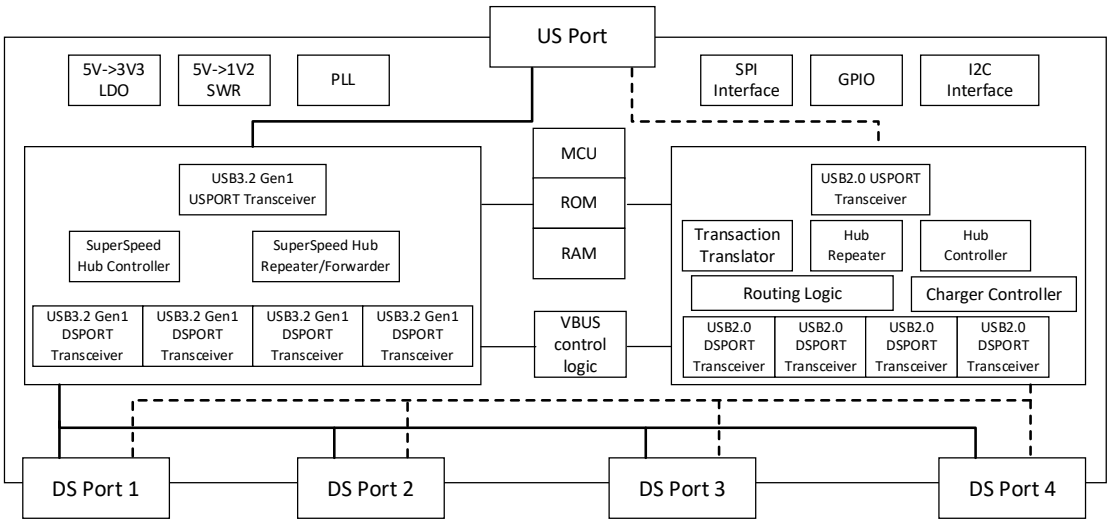
RESETN	24	I	External reset input, Active low. When RESETN = low, whole chip is reset to the initial state

SPI Interface			
Pin Name	**Pin Number**	**I/O**	**Description**
SPI_CLK	29	I/O	For SPI flash clock
SPI_CS	31	O	For SPI flash chip select
SPI_MOSI	28	I/O	For SPI flash data input
SPI_MISO	30	I/O	For SPI flash data output

Miscellaneous Interface			
Pin Name	**Pin Number**	**I/O**	**Description**
RTERM	16	I	Connect an external resistor (12K ±1%) to the Reference GND
NC	55		Not Connect

4. Function Description

4.1 Functional Block Diagram



4.2 Battery Charging

For the Battery Charger function, an external power supply is required. Otherwise, it will affect the power supply capability of the Battery Charger.

When HUB upstream port is connected, HUB downstream ports support BC1.2 CDP mode.

When HUB upstream port is not connected, HUB downstream ports support BC1.2 DCP mode and Apple/Galaxy charging mode.

4.3 LED Control

BGS3510S uses PLED pin to control the LED. It controls the LED lighting according to the flow

defined in Section 11.5.3 of Universal Serial Bus Specification Revision2.0. Both manual mode and Automatic mode are supported.
When BGS3510S connects to USB host, the LED will be turned on to indicate that a usb connection has been established. When BGS3510S is globally suspended or over current occurs, the LED will be turned off to save power.
As PLED is also used as configure GPIO(FN_C), the polarity of LED should be noticed.
Refer to Section 3.2 and BGS3510S schematic for detail.

With external SPI flash, BGS3510S supports LED customized control.

4.4 SPI flash interface

The BGS3510S will first check whether there is a valid firmware in external SPI Flash. If there is a valid firmware, BGS3510S will operate from external SPI flash. If not, BGS3510S will operate from internal ROM.

Requirement for SPI flash size

	Min
SPI flash size	1M bit

Requirement for SPI flash Command Support

Command Name	Command Code	Support Description
Read Status Register	05H	Must
Read Data	03H	Must
Fast Read	0BH	Must
Fast Read Dual Output	3BH	Optional
Write Enable	06H	Must
Write Disable	04H	Must
Page Program	02H	Must
Sector Erase	20H	Must
Block Erase(64K)	D8H	Must
Chip Erase	C7H	Must
Read Identification	9FH	Optional

4.5 I2C master interface

BGS3510S supports I2C master interface. The I2C master interface is default disabled after power on reset. It can be enabled when firmware running at external SPI flash.

The interface follows the I^2C-bus specification Rev.6, with support for the standard mode (100 kHz) and the fast mode (400 kHz) frequencies. Both the SCL and SDA signals require external pull-up resistors based on the specification. The SCL and SDA is 3.3V IO.

I2C master feature

- 7-bit addressing

- 7-bit combined format transfers
- Multiple Master Arbitration
- Clock synchronization
- Clock stretching

For details on I²C master operation, refer to I²C-bus specification and BGS3510S I²C master application guide.

4.6 I2C slave interface

BGS3510S supports I2C slave interface. The I2C slave interface is default disabled after power on reset. It can be enabled when firmware running at external SPI flash.

The interface follows the I²C-bus specification Rev.6, with support up to 100 kHz frequency. Both the SCL and SDA signals require external pull-up resistors based on the specification. The SCL and SDA is 3.3V IO.

I2C slave feature

- 7-bit addressing
- 7-bit combined format transfers
- Clock stretching

For details on I²C slave operation, refer to I²C-bus specification and BGS3510S I²C slave application guide.

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Note
V5	5V Power supply voltage	-0.5	6.0	V	
V_{33}	3.3V Power supply voltage	-0.5	3.6	V	
V_{12}	1.2V Power supply voltage	-0.5	1.32	V	
V_{IN}(1)	Input voltage at USB signal pins: TXN_P0~4/TXP_P0~4/ RXN_P0~4/RXP_P0~4/	-0.5	V_{12}+0.2	V	
	DM_P0~4/ DP_P0~4	-0.5	V_{33}+0.3	V	
	Input voltage at 5V tolerance I/O pins: FN_A/ FN_B/FN_C/ VBUS_DET/PWREN/OVCUR	-0.5	5.5	V	
	Input voltage at other I/O pins	-0.5	V_{33}+0.3	V	
Vout(2)	Output voltage	-0.5	V_{33}+0.3	V	
I_O(3)	Output current		6	mA	4mA type
			12	mA	8mA type

V_{ESD}	Electrostatic discharge	-4000	4000	V	Human Body Model (HBM)
		-500	500	V	Charged device model (CDM)
		-150	150	V	Machine Model (MM)
T_{STG}	Storage Temperature	-55	100	°C	

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(1) The absolute voltage range of power when power is applied to an input pin.

(2) The absolute voltage range of power when power is applied to an output pin.

(3) The absolute tolerance values for DC current when current flows out of or into output pin. The output driving strength of all output is 4mA by default, which can be configured as 8mA.

5.2 Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V5	5V Power supply voltage	4.75	5.0	5.25	V
V_{33}	3.3V Power supply voltage	3.0	3.3	3.6	V
V_{12}	1.2V Power supply voltage	1.15	1.2	1.32	V
T_A	Ambient temperature	0	-	70	°C
T_J	Absolute maximum junction temperature	0	-	125	°C

5.3 DC Characteristics

5.3.1 DC Characteristics except USB Signals

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	-	-	1.1	V
V_{IH}	Input High Voltage	1.7	-	-	V
V_{OL}	Output Low Voltage when I_{OL}=8mA	-	-	0.3	V
V_{OH}	Output High Voltage when I_{OH}=8mA	2.9	-	-	V
I_{IL}	Input Leakage Current			5	μA
R_{DN}	Pad internal pull down resister		180		KΩ
R_{UP}	Pad internal pull up resister		160		KΩ

5.3.2 USB 2.0 Interface DC Characteristics

BGS3510S conforms to DC characteristics for Universal Serial Bus specification rev. 2.0.
Refer to the specification for more information.

5.3.3 USB 3.0 Interface DC Characteristics

BGS3510S conforms to DC characteristics for Universal Serial Bus 3.1 specification.
Refer to the specification for more information.

5.4 AC Characteristics

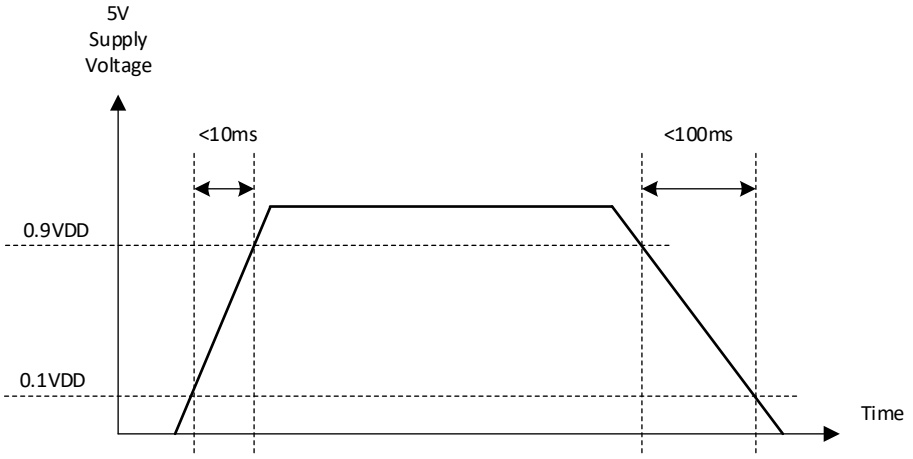
The following specifications apply when power supply voltages and operating temperature are within the recommended operating conditions in section 5.2.

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{CLK}	Crystal clock frequency	-100ppm	12	100ppm	MHz

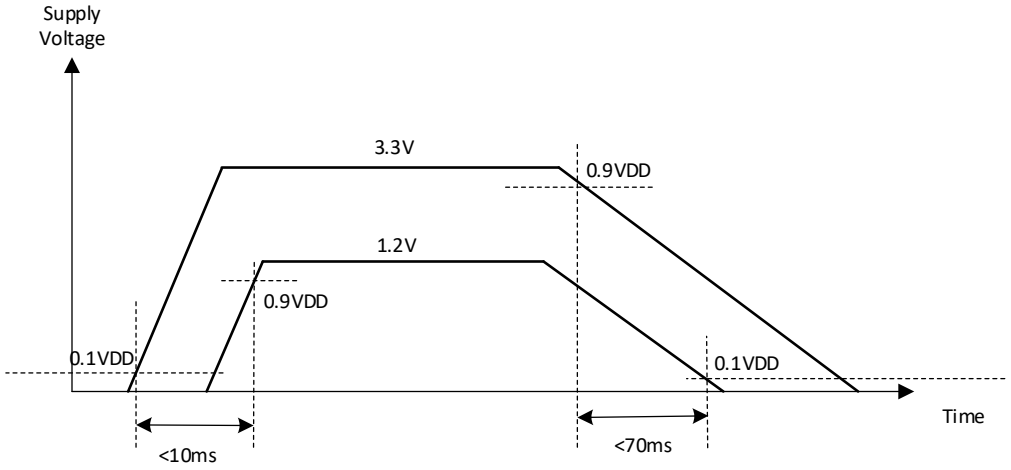
5.5 Power On/Off Timing

Only 5V power is need to power up BGS3510S when internal 5V to 3.3V LDO and internal 3.3V to 1.2V LDO are used. BGS3510S is powered up when the 5V power voltage is within the recommended operating range. It is powered down when the voltage is below that range, either stable or in transition.

The rising time of 5V power should be less than 10ms. And the falling time 5V power should be less than 100ms.



External 3.3V and 1.2V power are need to power up BGS3510S when internal 5V to 3.3V LDO and internal 3.3V to 1.2V LDO are not used. The voltage of 3.3V power should be always above the 1.2V power. Refer to Figure for detail



5.6 Input Clock Requirement

When using an external clock source such as an oscillator, the reference clock should have a ±100 PPM or better frequency stability and have less than 50-ps absolute peak to peak jitter or less than

25-ps peak to peak jitter after applying the USB 3.0 jitter transfer function.
XI should be tied to the 3.3V clock source and XO should be left floating.
Input clock amplitude range: (2.5V, 3.3V]

5.7 Reset Timing

BGS3510S's power on reset can either be triggered by external reset or internal power good reset circuit. BGS3510S's internal reset is designed to monitor silicon's internal power and initiate reset when unstable power event occurs. The power on sequence will start after the power good voltage has been met, and the reset will be released after approximately 10ms after power good.
To fully control the reset process of BGS3510S, the reset time applied in the external reset circuit should longer than that of the internal reset circuit.
Timing of POR is illustrated as below figure.

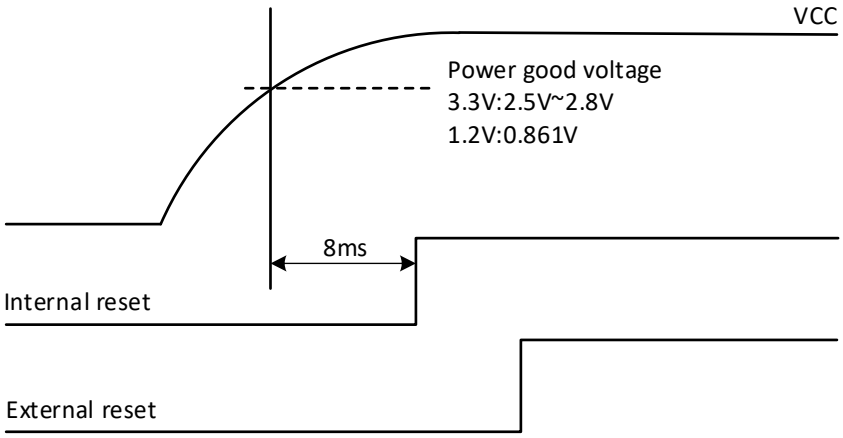


Figure Timing of Power On Reset

5.8 Power Consumption

The following table shows the power consumed in 5V domain.
BGS3510S integrates 5V to 3.3V and 5V to 1.2V regulators. If supplying 5V power, internal regulators convert 5V to 3.3V and 1.2V. And the power in the following table includes 1.2V and 3.3V power consumption and conversion loss.

Device Connection	Condition	5V Supply Current (mA)	Power (mW)
No host connection	Hub is not connected to host controller.	0.83	4.15
Suspend	Hub is connected to host controller both with SuperSpeed and HighSpeed, hub USB3 goes into U3 state, hub usb2 goes into L2 state.	3.35	16.75
1 HS device	Hub is connected to host controller both with SuperSpeed and HighSpeed, hub USB3 goes into U3 state. High-Speed data transfer on one port.	30.90	153.26
2 HS device	Hub is connected to host controller both with SuperSpeed and HighSpeed, hub USB3 goes into U3 state. High-Speed data transfer on two ports.	39.00	193.05

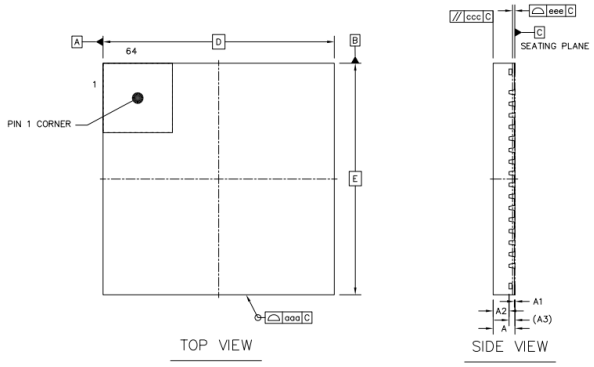
3 HS device	Hub is connected to host controller both with SuperSpeed and HighSpeed, hub USB3 goes into U3 state. High-Speed data transfer on three ports.	47.70	235.64
4 HS device	Hub is connected to host controller both with SuperSpeed and HighSpeed, hub USB3 goes into U3 state. High-Speed data transfer on four ports.	57.20	282.00
1 SS device	Hub is connected to host controller both with SuperSpeed and HighSpeed, hub USB2 goes into L2 state. Super-Speed data transfer on one port.	70.80	349.04
2 SS device	Hub is connected to host controller both with SuperSpeed and HighSpeed, hub USB2 goes into L2 state. Super-Speed data transfer on two ports.	89.30	438.46
3 SS device	Hub is connected to host controller both with SuperSpeed and HighSpeed, hub USB2 goes into L2 state. Super-Speed data transfer on three ports.	107.30	536.50
4 SS device	Hub is connected to host controller both with SuperSpeed and HighSpeed, hub USB2 goes into L2 state. Super-Speed data transfer on four ports.	127.20	633.46
4 SS device + 4 HS device	Hub is connected to host controller both with SuperSpeed and HighSpeed. Super-Speed data transfer on four ports, and High-Speed data transfer on four ports.	180.00	891.00

Note:

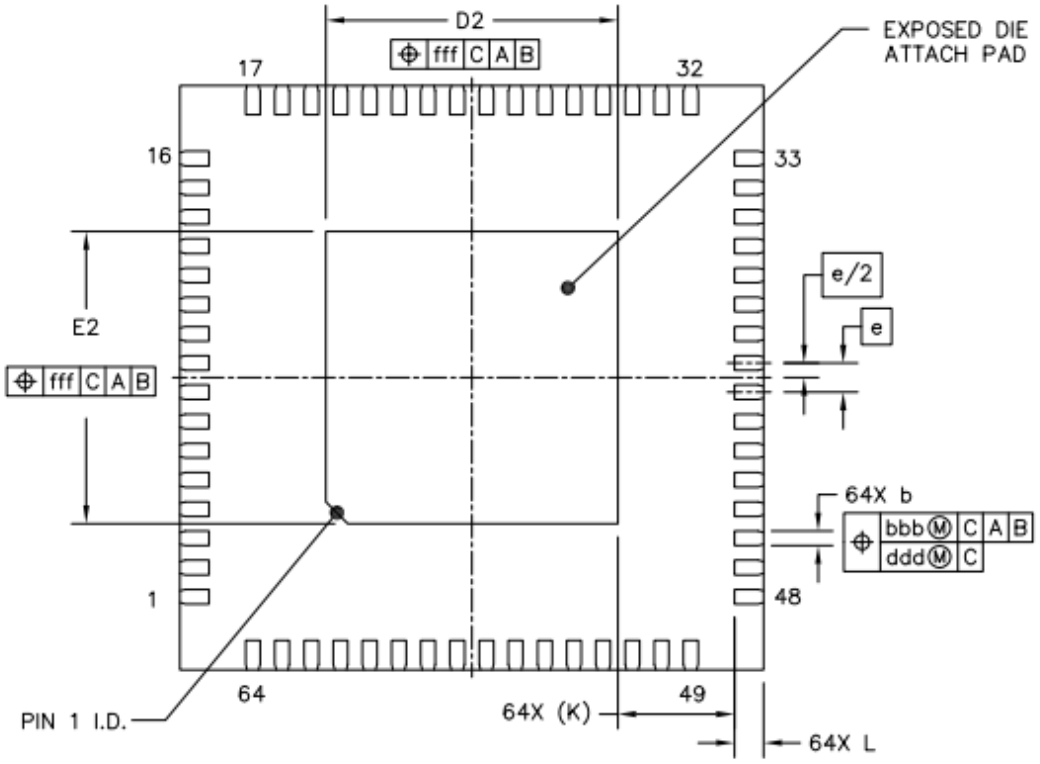
(1) The table does not include the current consumption of charger function.

(2) The table does not include the addition current consumption contributed by external circuits connect to GPIOs.

6. Package Dimension



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		8 BSC	
	Y	E		8 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	D2	3.9	4	4.1
	Y	E2	3.9	4	4.1
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		1.6 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.07	
		ddd		0.05	
EXPOSED PAD OFFSET		fff		0.1	



BOTTOM VIEW