BGS3501
USB2.0 High Speed Hub Controller

Datasheet

Revision 1.00

Feb. 18, 2024

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Revision History

Revision	Date	Description
1.00	02/18/2024	First release

Table of Contents

1. General Description

BGS3501 is a USB2.0 High Speed 4-port HUB controller which is compliant with USB2.0 specification. It is fully backward compatible to USB1.1 specification.

BGS3501 integrates self-developed USB 2.0 High-Speed PHY which has good signal integrity and compatibility. It also integrates 5V to 3.3V and 3.3V to 1.2V regulators which could the reduce BOM cost and ease the PCB design.

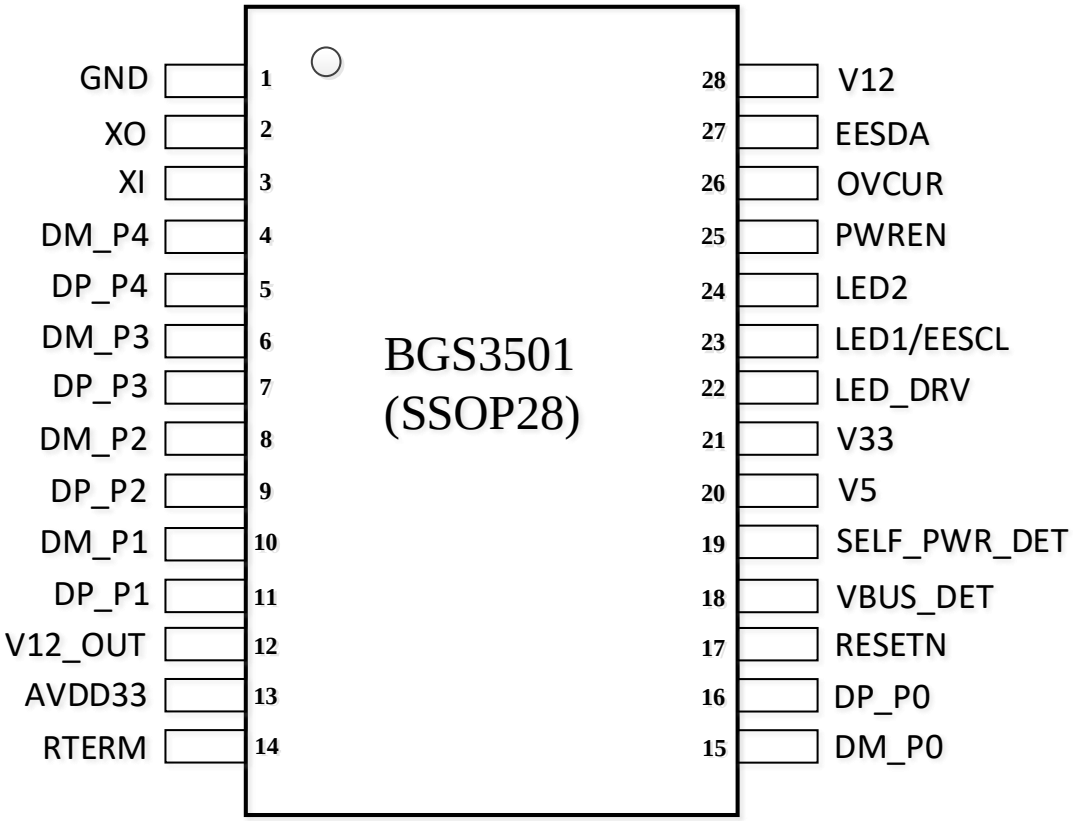
BGS3501 supports battery charging function for all downstream ports. It is compliant with USB Battery Charging specification rev1.2.

2. Features

- Compliant with USB 2.0 Specification Revision 2.0
  - Upstream port supports High-Speed and Full-Speed traffic
  - 4 downstream ports support High-Speed, Full-Speed, and Low-Speed traffic
  - 1 control pipe and 1 interrupt pipe
  - Backward compatible to USB specification Revision 1.1
- Advanced power management and low power consumption
  - Support USB2.0 Link Power Management (LPM) L0/L2
- STT(Single Transaction Translator)
  - One TT for all downstream ports for more cost effective
- Compliant with USB Battery Charging Specification Revision 1.2
  - Support BC1.2 Charging Downstream Port (CDP) mode
  - Support BC1.2 Dedicated Charging Port (DCP) mode
- Flexible design
  - Support Poly-fuse mode and Power Switch mode
  - Support LED blinking
- Configurable settings
  - Support Efuse for function configure
  - Support external EEPROM for function configure
- Low BOM cost
  - Single external 12 MHz crystal
  - Built-in upstream port 1.5KΩ pull-up and downstream port 15KΩ pull-down resistors
  - Built-in 5V to 3.3V and 3.3V to 1.2V regulator
- Application
  - USB hub/Docking station
  - Monitors/TV
  - Computer Systems
  - Set-Top Boxes

3. Pin Assignment

3.1 Pin-out Diagram



3.2 Pin Descriptions

Signal Type Definition

Name	Type	Description
Input	I	input-only signal
Output	O	output-only signal
Input/Output	I/O	bi-directional signal
Power	P	power/ground

Power/Ground Interface			
Pin Name	**Pin Number**	**I/O**	**Description**
GND	1	P	Ground
V12_OUT	12	P	3.3V to 1.2V regulator 1.2V output
AVDD33	13	P	3.3V power input for analog circuit
V12	28	P	1.2V power input
V33	21	P	5V to 3.3V regulator 3.3V output and 3.3 input
V5	20	P	5V power input

USB2.0 Interface			
Pin Name	**Pin Number**	**I/O**	**Description**
DM_P0 DP_P0	15 16	I/O	USB 2.0 DM/DP for Upstream Port
DM_P1 DP_P1	10 11	I/O	USB 2.0 DM/DP for Downstream Port1
DM_P2 DP_P2	8 9	I/O	USB 2.0 DM/DP for Downstream Port2
DM_P3 DP_P3	6 7	I/O	USB 2.0 DM/DP for Downstream Port3
DM_P4 DP_P4	4 5	I/O	USB 2.0 DM/DP for Downstream Port4

Hub Interface			
Pin Name	**Pin Number**	**I/O**	**Description**
PWREN	25	I/O	1. PWREN is the only power-enable output for GANG mode. 2. Strapping for Power Switch or Poly Fuse • Pull high to support low-active power switch • Floating to support poly-fuse • Pull down to support high-active power switch
OVCUR	26	I/O	OVCUR is the only over current flag for GANG mode
VBUS_DET	18	I	Upstream VBUS power detection pin. Active High.
SELF_PWR_DET	19	I	External power detection pin. High Active.

Clock and Reset Interface			
Pin Name	**Pin Number**	**I/O**	**Description**
XI	3	I	12M Crystal input. This pin is the crystal input for the internal oscillator. The input may alternately be driven by the output of an external oscillator. When using a crystal, a 1-MΩ feedback resistor is required between XI and XO.
XO	2	O	12M Crystal output. This pin is the crystal output for the internal oscillator. If XI is driven by an external oscillator this pin may be left unconnected. When using a crystal, a 1-MΩ feedback resistor is required between XI and XO.
RESETN	17	I	External reset input, Active low. When low, whole chip is reset to the initial state

GPIO Interface			
Pin Name	**Pin Number**	**I/O**	**Description**
EESDA	27	I/O	External Serial EEPROM Data/Address
LED1/EESCL	23	I/O	LED control (1) / external Serial EEPROM Clock (2)
LED2	24	I/O	LED control(1)
LED_DRV	22	I/O	LED Drive Control(1)

Note:

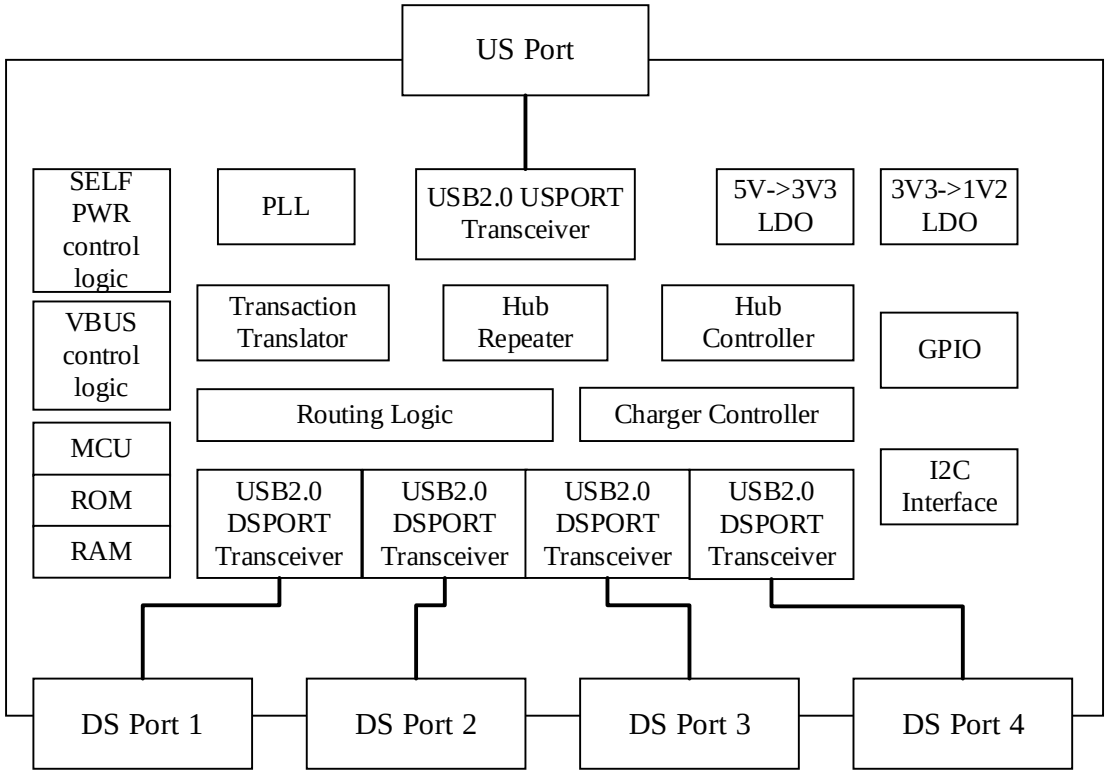
(1), LED1/LED2/LED_DRV work together on the LED control.

(2), After power on, BGS3501 first loads configure data from external EEPROM if EEPROM is existed, and then change GPIO to LED control function.

Miscellaneous Interface			
Pin Name	**Pin Number**	**I/O**	**Description**
RTERM	14	I	Connect an external resistor (12K ±1%) to the Reference GND

4. Function Description

4.1 Functional Block Diagram



4.2 Battery Charging

For the Battery Charger function, an external power supply is required. Otherwise, it will affect the power supply capability of the Battery Charger.

When HUB upstream port is connected, HUB downstream ports support BC1.2 CDP mode.

When HUB upstream port is not connected, HUB downstream ports support BC1.2 DCP mode.

4.3 LED Control

BGS3501 uses LED_DRV/LED1/LED2 pins to control the 5 LED function.
One of LEDs corresponds to hub upstream port state;
The four LEDs correspond to four downstream port states respectively.

	Upstream Port LED Status
Hub upstream connect to USB host successfully	On
Hub upstream port disconnect	Off
Hub is at suspend state	Off

	Downstream Port LED Status
Device connects successfully at downstream port	On
No Device at downstream port	Off
Device at downstream port is at suspend state	Off

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Note
V5	5V Power supply voltage	-0.5	6.0	V	
V_{33}	3.3V Power supply voltage	-0.5	3.6	V	
V_{12}	1.2V Power supply voltage	-0.5	1.32	V	
V_{IN}(1)	DM_P0~4/ DP_P0~4	-0.5	V_{33}+0.3	V	
	Input voltage at 5V tolerance I/O pins: PWREN/OVCUR/ VBUS_DET/ SELF_PWR_DET/LED2	-0.5	5.5	V	
	Input voltage at other I/O pins	-0.5	V_{33}+0.3	V	
Vout(2)	Output voltage	-0.5	V_{33}+0.3	V	
I_O(3)	Output current		6	mA	4mA type
			12	mA	8mA type
V_{ESD}	Electrostatic discharge	-4000	4000	V	Human Body Model (HBM)
		-500	500	V	Charged device model (CDM)
		-150	150	V	Machine Model (MM)
T_{STG}	Storage Temperature	-55	100	ºC	

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(1) The absolute voltage range of power when power is applied to an input pin.

(2) The absolute voltage range of power when power is applied to an output pin.

(3) The absolute tolerance values for DC current when current flows out of or into output pin. The output driving strength of all output is 4mA by default, which can be configured as 8mA.

5.2 Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V5	5V Power supply voltage	4.75	5.0	5.25	V
V_{33}	3.3V Power supply voltage	3.0	3.3	3.6	V
V_{12}	1.2V Power supply voltage	1.15	1.2	1.32	V
T_A	Ambient temperature	0	-	70	°C
T_J	Absolute maximum junction temperature	0	-	125	°C

5.3 DC Characteristics

5.3.1 DC Characteristics except USB Signals

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	-	-	1.1	V
V_{IH}	Input High Voltage	1.7	-	-	V
V_{OL}	Output Low Voltage when I_{OL}=8mA	-	-	0.3	V
V_{OH}	Output High Voltage when I_{OH}=8mA	2.9	-	-	V
I_{IL}	Input Leakage Current			5	μA
R_{DN}	Pad internal pull down resister		180		KΩ
R_{UP}	Pad internal pull up resister		160		KΩ

5.3.2 USB 2.0 Interface DC Characteristics

BGS3501 conforms to DC characteristics for Universal Serial Bus specification rev. 2.0.
Refer to the specification for more information.

5.4 AC Characteristics

The following specifications apply when power supply voltages and operating temperature are within the recommended operating conditions in section 5.2.

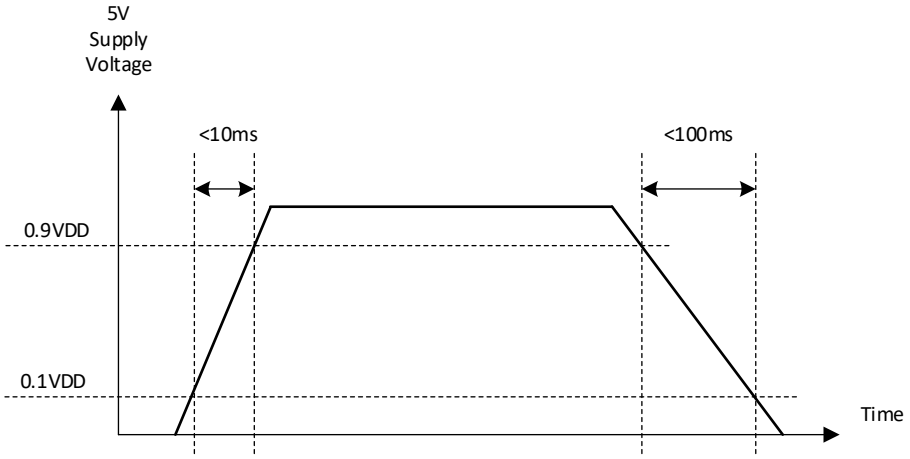
Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{CLK}	Crystal clock frequency	-100ppm	12	100ppm	MHz

5.5 Power On/Off Timing

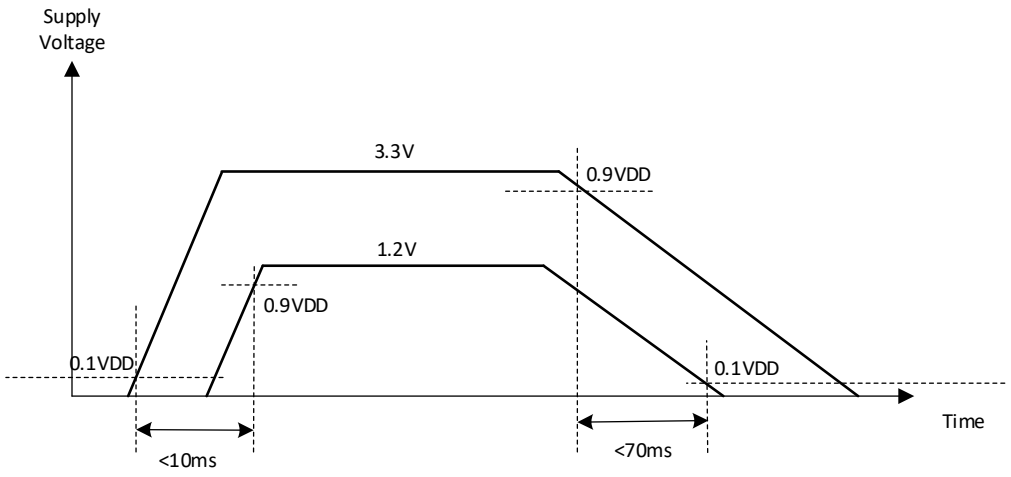
Only 5V power is need to power up BGS3501 when internal 5V to 3.3V LDO and internal 3.3V to 1.2V LDO are used. BGS3501 is powered up when the 5V power voltage is within the recommended

operating range. It is powered down when the voltage is below that range, either stable or in transition.

The rising time of 5V power should be less than 10ms. And the falling time 5V power should be less than 100ms.



External 3.3V and 1.2V power are need to power up BGS3501 when internal 5V to 3.3V LDO and internal 3.3V to 1.2V LDO are not used. The voltage of 3.3V power should be always above the 1.2V power. Refer to Figure for detail



5.6 Input Clock Requirement

When using an external clock source such as an oscillator, the reference clock should have a ±100 PPM or better frequency stability and have less than 50-ps absolute peak to peak jitter or less than 25-ps peak to peak jitter after applying the USB 3.0 jitter transfer function.

XI should be tied to the 3.3V clock source and XO should be left floating.

Input clock amplitude range: (2.5V, 3.3V]

5.7 Reset Timing

BGS3501's power on reset can either be triggered by external reset or internal power good reset circuit. BGS3501's internal reset is designed to monitor silicon's internal power and initiate reset when unstable power event occurs. The power on sequence will start after the power good voltage has been met, and the reset will be released after approximately 10ms after power good.

To fully control the reset process of BGS3501, the reset time applied in the external reset circuit should longer than that of the internal reset circuit.
Timing of POR is illustrated as below figure.

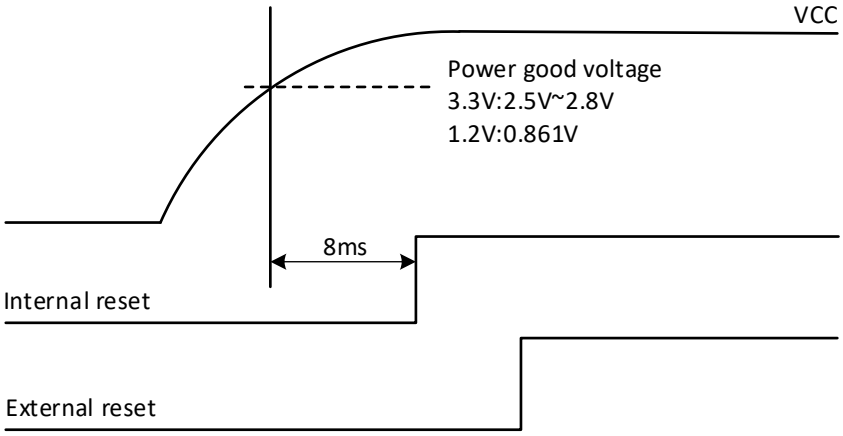
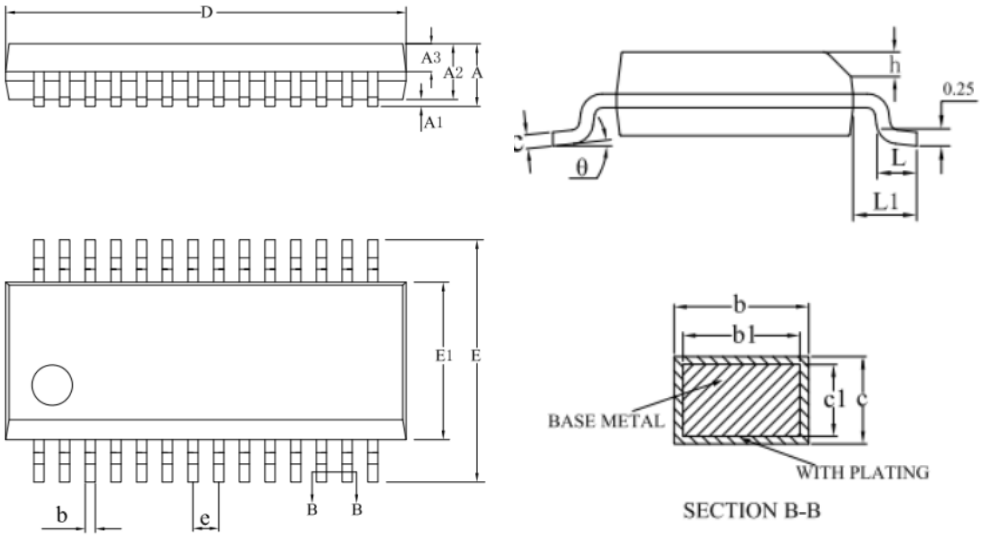


Figure Timing of Power On Reset

6. Package Dimension



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.05	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.23	—	0.31
b1	0.22	0.25	0.28
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.635BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05BSC		
θ	0°	—	8°