BGS3523
USB3.2 Gen1x1 Hub Controller

Datasheet

Revision 1.00

Aug. 13, 2024

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Revision History

Revision	Date	Description
1.00	13/08/2024	Initial Version

Table of Contents

1. General Description

BGS3523 is a USB3.2 Gen1x1 4-port HUB controller which is compliant with USB3.2 specification. It is fully backward compatible to USB2.0 and USB1.1 specification.

BGS3523 integrates self-developed USB 3.2 Gen 1x1 Super Speed transmitter/receiver physical layer (PHY) and USB 2.0 High-Speed PHY which has good signal integrity and compatibility. It also integrates 5V to 3.3V and 5V to 1.2V regulators which could the reduce BOM cost and ease the PCB design.

BGS3523 supports battery charging function for all downstream ports. It is compliant with USB Battery Charging specification rev1.2 and supports charging various portable devices, such as Apple, Samsung Galaxy devices.

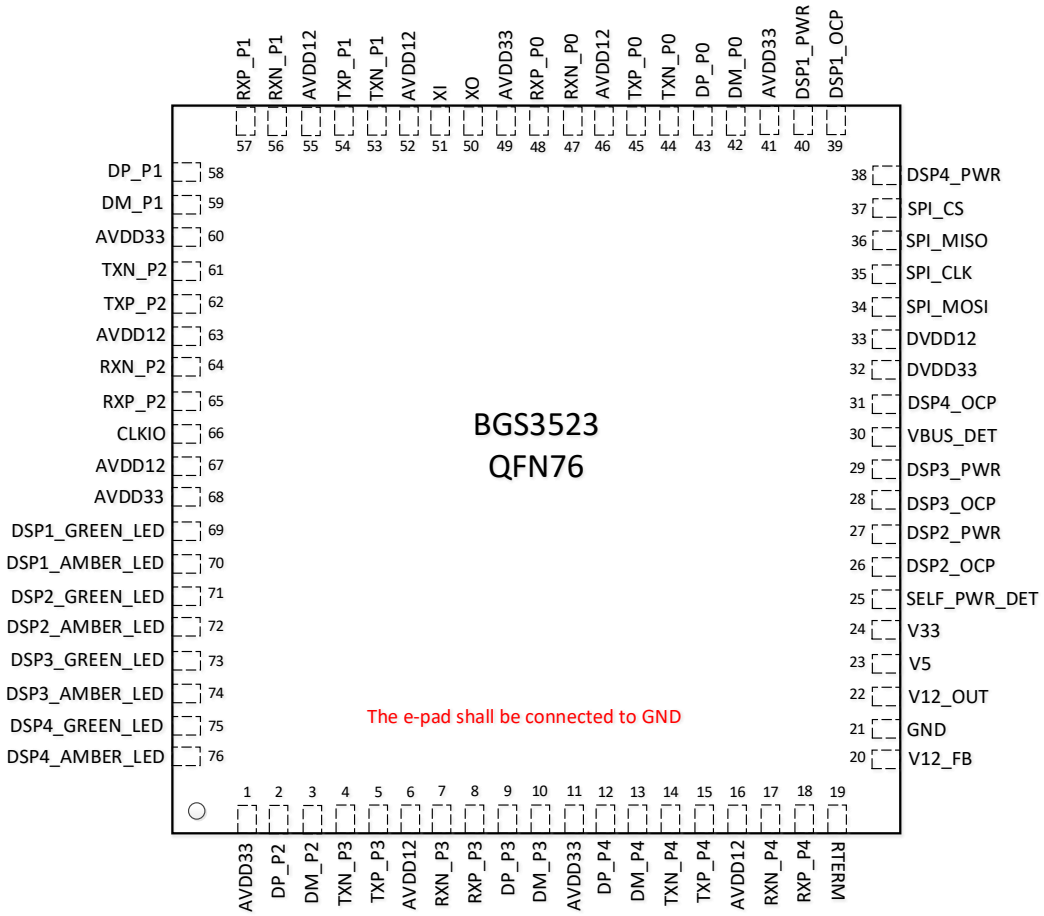
BGS3523 supports several interfaces, such as GPIOs and SPI. With these interfaces, BGS3523 supports a variety of applications. And it provides a framework for in-field firmware update and supports various customizations by updating firmware in external SPI flash.

2. Features

- Compliant with USB 3.2 Specification Revision 1.0
  - Upstream port supports Super-Speed, High-Speed and Full-Speed traffic
  - 4 downstream ports support Super-Speed, High-Speed, Full-Speed, and Low-Speed traffic
  - 1 control pipe and 1 interrupt pipe
  - Backward compatible to USB specification Revision 2.0 and 1.1
- Advanced power management and low power consumption
  - Support USB 3.2 Gen1x1 U0/U1/U2/U3 power management states
  - Support USB2.0 Link Power Management (LPM) L0/L1/L2
- MTT(Multiple Transaction Translator)
  - One TT for each downstream port.
  - Better data throughput when multiple downstream ports act on Full-Speed/Low-Speed concurrently.
- Compliant with USB Battery Charging Specification Revision 1.2 and other portable devices
  - Support BC1.2 Charging Downstream Port (CDP) mode
  - Support BC1.2 Dedicated Charging Port (DCP) mode
  - Support Apple 1A/2.1A/2.4A Charger mode (Divider Mode)
  - Support Samsung Galaxy devices fast-charging
- Flexible design
  - Support Poly-fuse mode and Power Switch mode
  - Support Gang Mode and Individual Mode
  - Support external SPI flash for firmware upgrade
  - Support LED customize control
  - On-chip 8bit micro-processor
- Configurable settings
  - Support Efuse for function configure
  - Support GPIO pull control at PCB for function configure
- Low BOM cost
  - Single external 12 MHz crystal
  - Built-in upstream port 1.5KΩ pull-up and downstream port 15KΩ pull-down resistors
  - Built-in 5V to 3.3V and 5V to 1.2V regulator
- Application
  - USB hub/Docking station
  - Monitors/TV
  - Computer Systems
  - Set-Top Boxes

3. Pin Assignment

3.1 Pin-out Diagram



3.2 Pin Descriptions

Signal Type Definition

Name	Type	Description
Input	I	input-only signal
Output	O	output-only signal
Input/Output	I/O	bi-directional signal
Power	P	power/ground

Power/Ground Interface			
Pin Name	**Pin Number**	**I/O**	**Description**
AVDD12	6,16,46,55,52,63,67	P	1.2V power input for analog circuit
DVDD12	33	P	1.2V power input for digital circuit
AVDD33	1,11,41,49,60,68	P	3.3V power input for analog circuit
DVDD33	32	P	3.3V power input for digital circuit
V33	24	P	5V-to-3.3V regulator 3.3V output and 3.3 input
V12_OUT	22	P	5V-to-1.2V DC-DC Switching regulator 1.2V output

V12_FB	20	P	5V-to-1.2V DC-DC Switching regulator feedback
V5	23	P	5V power input
GND	21	P	Ground

USB3.2 GEN1x1 Interface			
Pin Name	**Pin Number**	**I/O**	**Description**
TXN_P0 TXP_P0	44 45	O	USB3.2 Gen1x1 Differential Data Transmitter TX-/TX+ of Upstream Port
RXN_P0 RXP_P0	47 48	I	USB3.2 Gen1x1 Differential Data Receiver RX-/RX+ of Upstream Port
TXN_P1 TXP_P1	53 54	O	USB3.2 Gen1x1 Differential Data Transmitter TX-/TX+ of Downstream Port1
RXN_P1 RXP_P1	56 57	I	USB3.2 Gen1x1 Differential Data Receiver RX-/RX+ of Downstream Port1
TXN_P2 TXP_P2	61 62	O	USB3.2 Gen1x1 Differential Data Transmitter TX-/TX+ of Downstream Port2
RXN_P2 RXP_P2	64 65	I	USB3.2 Gen1x1 Differential Data Receiver RX-/RX+ of Downstream Port2
TXN_P3 TXP_P3	4 5	O	USB3.2 Gen1x1 Differential Data Transmitter TX-/TX+ of Downstream Port3
RXN_P3 RXP_P3	7 8	I	USB3.2 Gen1x1 Differential Data Receiver RX-/RX+ of Downstream Port3
TXN_P4 TXP_P4	14 15	O	USB3.2 Gen1x1 Differential Data Transmitter TX-/TX+ of Downstream Port4
RXN_P4 RXP_P4	17 18	I	USB3.2 Gen1x1 Differential Data Receiver RX-/RX+ of Downstream Port4

USB2.0 Interface			
Pin Name	**Pin Number**	**I/O**	**Description**
DM_P0 DP_P0	42 43	I/O	USB 2.0 DM/DP for Upstream Port
DM_P1 DP_P1	59 58	I/O	USB 2.0 DM/DP for Downstream Port1
DM_P2 DP_P2	3 2	I/O	USB 2.0 DM/DP for Downstream Port2
DM_P3 DP_P3	10 9	I/O	USB 2.0 DM/DP for Downstream Port3
DM_P4 DP_P4	13 12	I/O	USB 2.0 DM/DP for Downstream Port4

Hub Interface

Pin Name	Pin Number	I/O	Description
DSP1_PWR	40	I/O	1. External power switch enable pin for downstream port1. 2. Strapping for Power Switch or PolyFuse • Pull high to support low-active power switch • Floating to support poly-fuse • Pull down to support high-active power switch
DSP1_OCP	39	I/O	Over Current Protection flag for downstream port1. Default active low.
DSP2_PWR	27	I/O	External power switch enable pin for downstream port2. Active level is same to downstream port1.
DSP2_OCP	26	I/O	Over Current Protection flag for downstream port2. Default active low.
DSP3_PWR	29	I/O	External power switch enable pin for downstream port3. Active level is same to downstream port1.
DSP3_OCP	28	I/O	Over Current Protection flag for downstream port3. Default active low.
DSP4_PWR	38	I/O	External power switch enable pin for downstream port4. Active level is same to downstream port1.
DSP4_OCP	31	I/O	Over Current Protection flag for downstream port4. Default active low.
VBUS_DET	30	I	Upstream VBUS power detection pin. Active High.
SELF_PWR_DET	25	I	Self power detection pin. Active High.

GPIO Interface			
Pin Name	**Pin Number**	**I/O**	**Description**
DSP1_GREEN_LED	69	I/O	1. Downstream Port1 Green (Port Connect) LED Indicator. Output high when active; 2. General Purpose I/O. Can be used as general purpose I/O when used with external SPI;
DSP1_AMBER_LED	70	I/O	1. Downstream Port1 Amber (Over Current) LED Indicator. Output high when active; 2. General Purpose I/O. Can be used as general purpose I/O when used with external SPI;
DSP2_GREEN_LED	71	I/O	1. Downstream Port2 Green (Port Connect) LED Indicator. Output high when active;

			2. General Purpose I/O. Can be used as general purpose I/O when used with external SPI;
DSP2_AMBER_LED	72	I/O	1. Downstream Port2 Amber (Over Current) LED Indicator. Output high when active; 2. General Purpose I/O. Can be used as general purpose I/O when used with external SPI; Indicator.
DSP3_GREEN_LED	73	I/O	1. Downstream Port3 Green (Port Connect) LED Indicator. Output high when active; 2. General Purpose I/O. Can be used as general purpose I/O when used with external SPI;
DSP3_AMBER_LED	74	I/O	1. Downstream Port3 Amber (Over Current) LED Indicator. Output high when active; 2. General Purpose I/O. Can be used as general purpose I/O when used with external SPI;
DSP4_GREEN_LED	75	I/O	1. Downstream Port4 Green (Port Connect) LED Indicator. Output high when active; 3. General Purpose I/O. Can be used as general purpose I/O when used with external SPI;
DSP4_AMBER_LED	76	I/O	1. Downstream Port4 Amber (Over Current) LED Indicator. Output high when active; 2. General Purpose I/O. Can be used as general purpose I/O when used with external SPI;

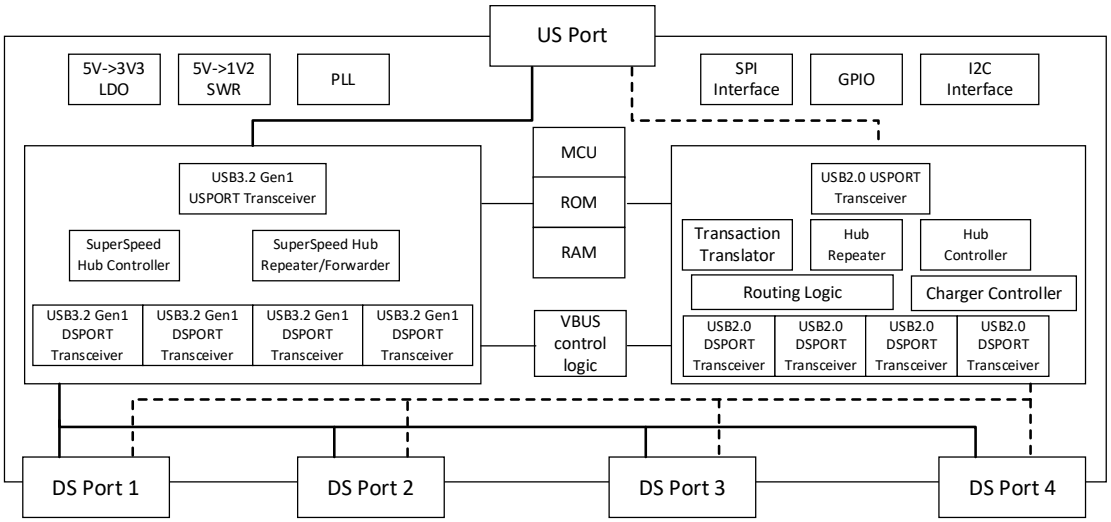
Clock Interface			
Pin Name	**Pin Number**	**I/O**	**Description**
XI	51	I	12M Crystal input. This pin is the crystal input for the internal oscillator. The input may alternately be driven by the output of an external oscillator. When using a crystal, a 1-MΩ feedback resistor is required between XI and XO.
XO	50	O	12M Crystal output. This pin is the crystal output for the internal oscillator. If XI is driven by an external oscillator this pin may be left unconnected. When using a crystal, a 1-MΩ feedback resistor is required between XI and XO.
SPI Interface			

Pin Name	Pin Number	I/O	Description
SPI_CLK	35	I/O	For SPI flash clock
SPI_CS	37	O	For SPI flash chip select
SPI_MOSI	34	I/O	For SPI flash data input
SPI_MISO	36	I/O	For SPI flash data output

Miscellaneous Interface			
Pin Name	**Pin Number**	**I/O**	**Description**
RTERM	19	I	Connect an external resistor (12K ±1%) to the Reference GND
CLKIO	66		12M clock output

4. Function Description

4.1 Functional Block Diagram



4.2 Battery Charging

For the Battery Charger function, an external power supply is required. Otherwise, it will affect the power supply capability of the Battery Charger.

When HUB upstream port is connected, HUB downstream ports support BC1.2 CDP mode.

When HUB upstream port is not connected, HUB downstream ports support BC1.2 DCP mode and Apple/Galaxy charging mode.

4.3 LED Control

Each downstream port has 2 LED pin to indicate the port status.

BGS3523 controls the LEDs lighting according to the flow defined in Section 11.5.3 of Universal Serial Bus Specification Revision2.0. Both manual mode and Automatic mode are supported.

When a device is connected to the downstream port, the corresponding green LED light will be turned on. And the amber LED light will be turned on when over-current condition is detected on the downstream port.

With external SPI flash, BGS3523 supports LED customized control.

4.4 SPI flash interface

The BGS3523 will first check whether there is a valid firmware in external SPI Flash. If there is a valid firmware, BGS3523 will operate from external SPI flash. If not, BGS3523 will operate from internal ROM.

Requirement for SPI flash size

	Min
SPI flash size	1M bit

Requirement for SPI flash Command Support

Command Name	Command Code	Support Description
Read Status Register	05H	Must
Read Data	03H	Must
Fast Read	0BH	Must
Fast Read Dual Output	3BH	Optional
Write Enable	06H	Must
Write Disable	04H	Must
Page Program	02H	Must
Sector Erase	20H	Must
Block Erase(64K)	D8H	Must
Chip Erase	C7H	Must
Read Identification	9FH	Optional

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Note
V5	5V Power supply voltage	-0.5	6.0	V	
V_{33}	3.3V Power supply voltage	-0.5	3.6	V	
V_{12}	1.2V Power supply voltage	-0.5	1.32	V	
V_{IN}(1)	Input voltage at USB signal pins: TXN_P0~4/TXP_P0~4/ RXN_P0~4/RXP_P0~4/	-0.5	V_{12}+0.2	V	
	DM_P0~4/ DP_P0~4	-0.5	V_{33}+0.3	V	
	Input voltage at 5V tolerance I/O pins: FN_A/ FN_B/FN_C/ VBUS_DET/PWREN/OVCUR	-0.5	5.5	V	
	Input voltage at other I/O pins	-0.5	V_{33}+0.3	V	

Vout(2)	Output voltage	-0.5	V_{33}+0.3	V	
I_O(3)	Output current		6	mA	4mA type
			12	mA	8mA type
V_{ESD}	Electrostatic discharge	-4000	4000	V	Human Body Model (HBM)
		-500	500	V	Charged device model (CDM)
		-150	150	V	Machine Model (MM)
T_{STG}	Storage Temperature	-55	100	°C	

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(1) The absolute voltage range of power when power is applied to an input pin.

(2) The absolute voltage range of power when power is applied to an output pin.

(3) The absolute tolerance values for DC current when current flows out of or into output pin. The output driving strength of all output is 4mA by default, which can be configured as 8mA.

5.2 Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V5	5V Power supply voltage	4.75	5.0	5.25	V
V_{33}	3.3V Power supply voltage	3.0	3.3	3.6	V
V_{12}	1.2V Power supply voltage	1.15	1.2	1.32	V
T_A	Ambient temperature	0	-	70	°C
T_J	Absolute maximum junction temperature	0	-	125	°C

5.3 DC Characteristics

5.3.1 DC Characteristics except USB Signals

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	-	-	1.1	V
V_{IH}	Input High Voltage	1.7	-	-	V
V_{OL}	Output Low Voltage when I_{OL}=8mA	-	-	0.3	V
V_{OH}	Output High Voltage when I_{OH}=8mA	2.9	-	-	V
I_{IL}	Input Leakage Current			5	μA
R_{DN}	Pad internal pull down resister		180		KΩ
R_{UP}	Pad internal pull up resister		160		KΩ

5.3.2 USB 2.0 Interface DC Characteristics

BGS3523 conforms to DC characteristics for Universal Serial Bus specification rev. 2.0.
Refer to the specification for more information.

5.3.3 USB 3.0 Interface DC Characteristics

BGS3523 conforms to DC characteristics for Universal Serial Bus 3.1 specification.
Refer to the specification for more information.

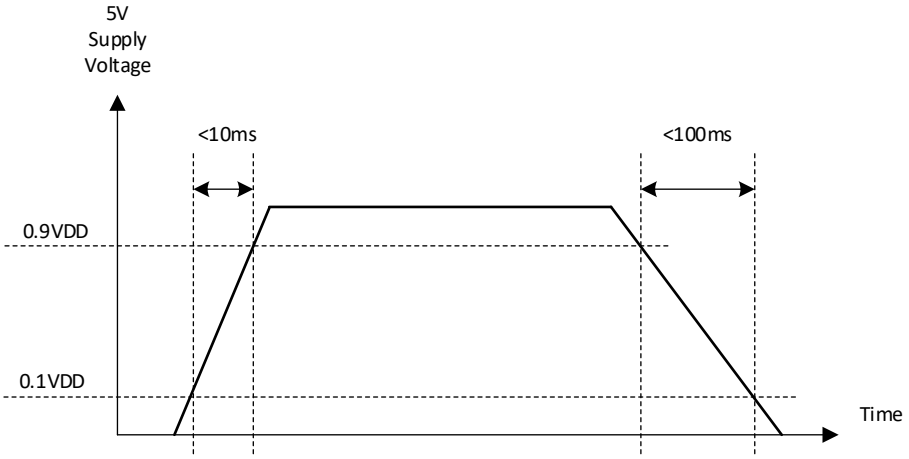
5.4 AC Characteristics

The following specifications apply when power supply voltages and operating temperature are within the recommended operating conditions in section 5.2.

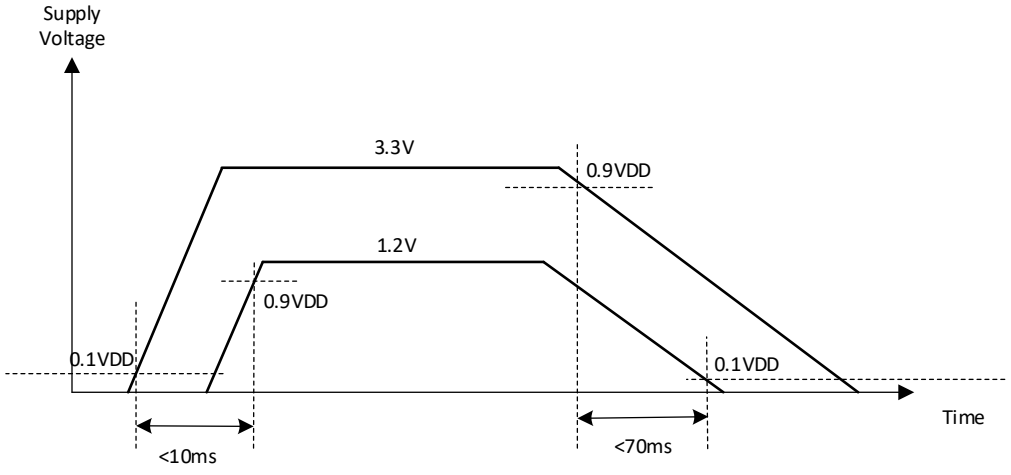
Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{CLK}	Crystal clock frequency	-100ppm	12	100ppm	MHz

5.5 Power On/Off Timing

Only 5V power is need to power up BGS3523 when internal 5V to 3.3V LDO and internal 3.3V to 1.2V LDO are used. BGS3523 is powered up when the 5V power voltage is within the recommended operating range. It is powered down when the voltage is below that range, either stable or in transition.
The rising time of 5V power should be less than 10ms. And the falling time 5V power should be less than 100ms.



External 3.3V and 1.2V power are need to power up BGS3523 when internal 5V to 3.3V LDO and internal 3.3V to 1.2V LDO are not used. The voltage of 3.3V power should be always above the 1.2V power. Refer to Figure for detail



5.6 Input Clock Requirement

When using an external clock source such as an oscillator, the reference clock should have a ±100 PPM or better frequency stability and have less than 50-ps absolute peak to peak jitter or less than 25-ps peak to peak jitter after applying the USB 3.0 jitter transfer function.
XI should be tied to the 3.3V clock source and XO should be left floating.
Input clock amplitude range: (2.5V, 3.3V]

6. Package Dimension